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10/754,483	01/09/2004	Kevin Conley	SDK1P017/503	6185

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOmail@beyerlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/754,483	CONLEY ET AL.	
	Examiner	Art Unit	
	YAIMA CAMPOS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/15/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/754,483, the examiner acknowledges the applicant's submission of the amendment dated 10/15/2009. At this point, claims 1-38 have been cancelled, and claims 39-62 have been added. Claims 39-62 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/15/2009 has been entered.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

3. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated 10/15/2009 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 39-62** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinomura (US 5,935,228) in view of Colligan et al. (US 6,519,762) and Suda (US 2004/0123059).

6. As per claim 39. (New) A method for reading data from a memory card that provides non-volatile data storage having an address space defined by a contiguous range of addresses, the method comprising: determining whether the non-volatile data storage utilizes a first file system or a second file system; **[Shinomura discloses "when a PC card that is driven only by a DOS/Windows 3.x compatible 16-bit device driver is inserted into a PC card slot of a computer system, the PC card is automatically enabled by a corresponding 16-bit device driver. And when a PC card that can be driven by a Windows 95 native mode 32-bit device driver is inserted into the computer system, the PC card is automatically enabled by a corresponding 32-bit device driver" (col. 10, line 61-col. 11, line 3) wherein "In general, an OS includes a "file manager" for managing the writing and reading of files" (col. 4, lines 10-11).** ***Thus, an operating system using a 16-bit driver comprises a corresponding 16-bit file system (interpreted as the claimed first file system) and an operating system using a 32-bit driver comprises a corresponding 32-bit file system; and determining whether a PC***

***card uses 16-bit driver or a 32-bit driver is interpreted as determining whether the memory card uses a first file system or a second file system*]** when the non-volatile data storage utilizes the first file system, operating the memory card in accordance with the first file system… formatting the memory card utilizing the first file system… and when the non-volatile data storage utilizes the second file system, operating the memory card in accordance with the second file system **[Shinomura teaches "the client device drivers 62 read card attribute information (tuple) from the memory in the PC card... In accordance with the contents of the tuple, each client device driver 62 ascertains whether it should drive the PC card" (col. 16, lines 5-9); when the tuple indicates a client device driver 62 may enable the PC card, the card in enabled by the client device driver 62 using 16-bit card service 61, in the DOS/Windows 3.x compatible mode (col. 11-26) and when the tuple indicates a client device driver 53 may enable the PC card, the PC card is enabled by the 32-bit card service 51, in the Windows 95 native mode (col. 16, lines 28-64) (See fig. 2 and related text);** ***therefore, when the memory card utilizes the 16-bit driver and corresponding 16-bit file system, it is formatted and operated in accordance with the 16-bit file system, and when the memory card utilizes the 32-bit driver and corresponding 32-bit file system, it is formatted and operated in accordance with the 32-bit file system*]**.

Shinomura does not expressly disclose the memory card is operated under the 16-bit driver and corresponding file system by "dividing the address space of the non-volatile data storage into a plurality of volumes; formatting each of the plurality of volumes as a separate volume utilizing the first file system; accessing one of the plurality of volumes by determining a position of a physical switch, wherein the position indicates

which of the plurality of volumes to access, wherein an offset is used to access volumes other than a first of the plurality of volumes;" nor when operating the memory card under the 32-bit driver and corresponding file system, "accessing the entire address space of the non-volatile data storage as the single volume".

Colligan discloses a non-volatile memory operated under a 16-bit file system by "dividing the address space of the non-volatile data storage into a plurality of volumes; formatting each of the plurality of volumes as a separate volume utilizing the first file system… wherein an offset is used to access volumes other than a first of the plurality of volumes" when operating the a non-volatile memory under a 32-bit file system, "accessing the entire address space of the non-volatile data storage as the single volume" as [**"For example, a 4.3 Gbyte hard disk drive 40 can include a single partition using the FAT 32 file type… For the FAT 32 file type, 4.2 Bbytes can be accessed per partition. For the FAT 16 file type, only 2.1 Gbytes per partition are allowed… For a similar 4.3 Gbyte hard disk drive 44 of FIG. 3 using a FAT 16 file type, however, the hard disk drive will contain multiple partitions (e.g. C: drive, D: drive and E: drive)" (See figs. 2-3 and related text; col. 8, lines 5-13);** ***wherein it is interpreted that since the hard drive operated under the FAT 16 or 16-bit file system comprises multiple partitions, the address space is divided into multiple partitions, and each partition is formatted as FAT 16 or 16-bit file system.*** **Figure 3 depicts the hard disk utilizing multiple partitions wherein the address range begins at "ADDR. 0" and ends at "ADDR. Max" wherein volumes 34 and 36 are shown, each beginning at an intermediate address within the address space, thus an offset must used from**

"ADDR. 0" in order to address and access volumes other than the first of the plurality of volumes (See fig. 3 and related text)].

Suda discloses a memory card ""accessing one of the plurality of volumes by determining a position of a physical switch, wherein the position indicates which of the plurality of volumes to access; wherein an offset is used to access volumes other than a first of the plurality of volumes" as **[a memory card comprising plural storage areas (Fig. 1 and related text) wherein "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028);** ***thus disclosing a memory card comprising plural storage areas which utilize a FAT 16 file system.*** **Suda further teaches "mechanical switches 16a and 16b for selecting one of the plural storage areas… It is possible to select any one of the storage areas… of the memory card… by use of mechanical switches… For example, when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches... thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2"… thereby allowing the memory card host device to handle the second storage area" (par. 0069; fig. 7 and related text);** ***thus determining which of a plurality of volumes to access based on a the position of a switch.*** **Suda further illustrates in figure 5, the address space of memory card beginning at address "00000" wherein a first storage area begins at address "00000," a second storage area begins at address "0FFFF" and a third storage area begins at address "1FFFF" and wherein the address space of the memory card ends at address "xFFFF;"** ***therefore in order to***

address the second storage area and the third storage area, an offset from address "00000" must be used **(fig. 5 and related text)]**.

Shinomura, Colligan and Suda are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system/method wherein it is determined whether a memory card utilizes a first file system/16-bit file system or a second file system/32-bit file system, formatting and operating the memory card according to the 16-bit file system when it is determined that the memory card utilized the 16-bit file system, and operating the card according to the 32-bit file system when it is determined that the memory card utilizes the 32-bit file system as taught by Shinomura, to divide the address space into multiple volumes when operating the memory card under the 16-bit file system, use an offset to access each of the plurality of volumes other than a first volume, and to operate the memory card as a single volume when the memory card utilized the 32-bit file system in the manner that Colligan teaches a memory device is operated as multiple partitions when utilizing a FAT-16 file system, or as a single partition when utilizing a FAT-32 file system since Colligan suggests this would **[enable efficient partitioning of the system into different areas according to the file system used (col. 8, lines 11-14)]**; and to further modify the combination of Shinomura and Colligan to access each of the plurality of volumes based on the position of a switch, wherein an offset is used to access each of the plurality of volumes other than then first volume as taught by Suda, since Suda discloses this would provide benefits as **["it is possible to switch storage areas without adding a new function to the memory card host device if a user designates the**

storage area by use of mechanical switches. Therefore, it is possible to use all the storage capacity included in the memory card." (par. 0070)].

Therefore, it would have been obvious to combine Shinomura with Colligan and Suda for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claim 39.

7. As per claim 40. (New) The method of claim 39, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[Shinomura discloses 16-bit addressing mode and 32-bit addressing mode (col. 7, lines 24-65). Colligan teaches FAT 16 file system and FAT 32 file system (col. 8, lines 1-16). Suda further teaches a memory card having plural area where each may utilizing a FAT 16 file system (par. 0028)]**.

8. As per claim 41. (New) The method of claim 39, wherein the first file system is the FAT-16 file system **[Shinomura discloses 16-bit addressing and 32-bit addressing (col. 7, lines 24-65). Colligan teaches FAT 16 file system and FAT 32 file system (col. 8, lines 1-16). Suda further teaches a memory card having plural area where each may utilizing a FAT 16 file system (par. 0028)]**.

9. As per claim 42. (New) The method of claim 39, wherein the second file system is the FAT-32 file system **[Shinomura discloses 16-bit addressing and 32-bit addressing (col. 7, lines 24-65). Colligan teaches FAT 16 file system and FAT 32 file system (col. 8, lines 1-16)]**.

10. As per claim 43. (New) The method of claim 40, wherein each of the plurality of volumes has a maximum size of 2GB **[Colligan teaches "For the FAT 16 file type, only 2.1 Gbytes per partition are allowed… the hard disk drive will contain multiple**

partitons" (col. 8, lines 11-16). Suda further teaches "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028); ***therefore, each FAT 16 or 16-bit file system storage area having a maximum size of 2 Gbytes*****]**.

11. As per claim 44. (New) The method of claim 39, wherein the determining includes accessing a portion of the non-volatile data storage stating which file system is utilized **[Shinomura discloses "the client device drivers 62 read card attribute information (tuple) from the memory in the PC card... In accordance with the contents of the tuple, each client device driver 62 ascertains whether it should drive the PC card" (col. 16, lines 5-9); when the tuple indicates a client device driver 62 may enable the PC card, the card in enabled by the client device driver 62 using 16-bit card service 61, in the DOS/Windows 3.x compatible mode (col. 11-26) and when the tuple indicates a client device driver 53 may enable the PC card, the PC card is enabled by the 32-bit card service 51, in the Windows 95 native mode (col. 16, lines 28-64) (See fig. 2 and related text);** ***thus accessing the tuple or a portion of the non-volatile memory stating whether 16-bit file system or 32-bit file system is utilized***].

12. As per claim 45. (New) A memory card comprising: non-volatile data storage that provides data storage having an address space; **[Shinomura discloses PC cards, each having address space (fig. 1 and related text)]**

a controller that manages access to the data stored in said non-volatile data storage, wherein the controller determines whether the non-volatile data storage utilizes a first file system or a second file system; **[Shinomura disclose "PC card controller 18" that**

manages access to PC card (col. 13, lines 9-23; fig. 1 and related text) comprising modules shown in (fig. 2) to perform the following functions: "when a PC card that is driven only by a DOS/Windows 3.x compatible 16-bit device driver is inserted into a PC card slot of a computer system, the PC card is automatically enabled by a corresponding 16-bit device driver. And when a PC card that can be driven by a Windows 95 native mode 32-bit device driver is inserted into the computer system, the PC card is automatically enabled by a corresponding 32-bit device driver" (col. 10, line 61-col. 11, line 3) wherein "In general, an OS includes a "file manager" for managing the writing and reading of files" (col. 4, lines 10-11). ***Thus, an operating system using a 16-bit driver comprises a corresponding 16-bit file system (interpreted as the claimed first file system) and an operating system using a 32-bit driver comprises a corresponding 32-bit file system; and determining whether a PC card uses 16-bit driver or a 32-bit driver is interpreted as determining whether the memory card uses a first file system or a second file system*****|***

wherein when the non-volatile data storage utilizes the first file system, the controller operates the memory card in accordance with the first file system… formatting the memory card utilizing the first file system… and wherein when the non-volatile data storage utilizes the second file system, the controller operates the memory card in accordance with the second file system **|Shinomura teaches "the client device drivers 62 read card attribute information (tuple) from the memory in the PC card... In accordance with the contents of the tuple, each client device driver 62 ascertains whether it should drive the PC card" (col. 16, lines 5-9); when the tuple indicates a client device driver 62 may enable the PC card, the card in enabled by the client**

device driver 62 using 16-bit card service 61, in the DOS/Windows 3.x compatible mode (col. 11-26) and when the tuple indicates a client device driver 53 may enable the PC card, the PC card is enabled by the 32-bit card service 51, in the Windows 95 native mode (col. 16, lines 28-64) (See fig. 2 and related text); ***therefore, when the memory card utilized the 16-bit driver and corresponding file system, it is formatted and operated in accordance with the 16-bit file system, and when the memory card utilizes the 32-bit driver and corresponding file system, it is formatted and operated in accordance with the 32-bit file system*****]**.

Shinomura does not expressly disclose "a switch being set in one of a plurality of switch positions," the memory card is operated under the 16-bit file system by "dividing the address space of the non-volatile data storage into a plurality of volumes; formatting each of the plurality of volumes as a separate volume utilizing the first file system; accessing one of the plurality of volumes by determining a position of a physical switch, wherein the position indicates which of the plurality of volumes to access, wherein an offset is used to access volumes other than a first of the plurality of volumes;" nor when operating the memory card under the 32-bit file system, "accessing the entire address space of the non-volatile data storage as the single volume".

Colligan discloses a non-volatile memory operated under a 16-bit file system by "dividing the address space of the non-volatile data storage into a plurality of volumes; formatting each of the plurality of volumes as a separate volume utilizing the first file system;… wherein an offset is used to access volumes other than a first of the plurality of volumes" when operating the a non-volatile memory under a 32-bit file system, "accessing the entire address space of the non-volatile data storage as the single volume"

as **["For example, a 4.3 Gbyte hard disk drive 40 can include a single partition using the FAT 32 file type… For the FAT 32 file type, 4.2 Bbytes can be accessed per partition. For the FAT 16 file type, only 2.1 Gbytes per partition are allowed… For a similar 4.3 Gbyte hard disk drive 44 of FIG. 3 using a FAT 16 file type, however, the hard disk drive will contain multiple partitions (e.g. C: drive, D: drive and E: drive)" (See figs. 2-3 and related text; col. 8, lines 5-13);** ***wherein it is interpreted that since the hard drive operated under the FAT 16 or 16-bit file system comprises multiple partitions, the address space is formatted and divided into multiple partitions.*** **Figure 3 depicts the hard disk utilizing multiple partitions wherein the address range begins at "ADDR. 0" and ends at "ADDR. Max" wherein volumes 34 and 36 are shown, each beginning at an intermediate address within the address space, thus an offset must used from "ADDR. 0" in order to address and access volumes other than the first of the plurality of volumes (See fig. 3 and related text)]**.

Suda discloses a memory card comprising "a switch being set in one of a plurality of switch positions;… accessing one of the plurality of volumes by determining a position of a physical switch, wherein the position indicates which of the plurality of volumes to access, wherein an offset is used to access volumes other than a first of the plurality of volumes" as **[a memory card comprising plural storage areas (Fig. 1 and related text) wherein "when a FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes… the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas" (par. 0028);** ***thus disclosing a memory card comprising plural storage areas which utilizes a FAT 16 file system.*** **Suda further teaches "mechanical switches 16a and 16b for**

selecting one of the plural storage areas… It is possible to select any one of the storage areas… of the memory card… by use of mechanical switches… For example, when the mechanical switches… are set to positions marked as "1," the controller 10 reflects the state of the switches... thereby allowing a memory card host device to handle the first storage area… when… set to position marked as "2"… thereby allowing the memory card host device to handle the second storage area" (par. 0069; fig. 7 and related text); ***thus determining which of a plurality of volumes to access based on a the position of a switch.*** **Suda further illustrates in figure 5, the address space of memory card beginning at address "00000" wherein a first storage area begins at address "00000," a second storage area begins at address "0FFFF" and a third storage area begins at address "1FFFF" and wherein the address space of the memory card ends at address "xFFFF;"** ***therefore in order to address the second storage area and the third storage area, an offset from address "00000" must be used*** **(fig. 5 and related text)].**

Shinomura, Colligan and Suda are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system/method wherein it is determined whether a memory card utilizes a first file system/16-bit file system or a second file system/32-bit file system, formatting and operating the memory card according to the 16-bit file system when it is determined that the memory card utilized the 16-bit file system, and operating the card according to the 32-bit file system when it is determined that the memory card utilizes the 32-bit file system as taught by Shinomura to divide the address space into

multiple volumes when operating the memory card under the 16-bit file system, use an offset to access each of the plurality of volumes other than a first volume, and to operate the memory card as a single volume when the memory card utilized the 32-bit file system in the manner that Colligan teaches a memory device is operated as multiple partitions when utilizing a FAT-16 file system, or as a single partition when utilizing a FAT-32 file system since Colligan suggests this would **[enable efficient partitioning of the system into different areas according to the file system used (col. 8, lines 11-14)]**; and to further modify the combination of Shinomura and Colligan to access each of the plurality of volumes based on the position of a switch, wherein an offset is used to access each of the plurality of volumes other than then first volume as taught by Suda, since Suda discloses this would provide benefits as **["it is possible to switch storage areas without adding a new function to the memory card host device if a user designates the storage area by use of mechanical switches. Therefore, it is possible to use all the storage capacity included in the memory card." (par. 0070)]**.

Therefore, it would have been obvious to combine Shinomura with Colligan and Suda for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claim 45.

13. As per claim 46. (New) The memory card of claim 45, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[The rationale in the rejection to claim 40 is herein incorporated]**.

14. As per claim 47. (New) The memory card of claim 45, wherein the first file system is the FAT-16 file system **[The rationale in the rejection to claim 41 is herein incorporated]**.

15. As per claim 48. (New) The memory card of claim 45, wherein the second file system is the FAT- 32 file system **[The rationale in the rejection to claim 42 is herein incorporated]**.

16. As per claim 49. (New) The memory card of claim 46, wherein each of the plurality of volumes has a maximum size of 2GB **[The rationale in the rejection to claim 43 is herein incorporated]**.

17. As per claim 50. (New) The memory card of claim 45, wherein the determining includes accessing a portion of the non-volatile data storage stating which file system is utilized **[The rationale in the rejection to claim 44 is herein incorporated]**.

18. As per claim 51. (New) An apparatus for reading data from a memory card that provides non-volatile data storage having an address space defined by a contiguous range of addresses, the apparatus comprising: means for determining whether the non-volatile data storage utilizes a first file system or a second file system; means for, when the non-volatile data storage utilizes the first file system, operating the memory card in accordance with the first file system by: dividing the address space of the non-volatile data storage into a plurality of volumes; formatting each of the plurality of volumes as a separate volume utilizing the first file system; accessing one of the plurality of volumes by determining a position of a physical switch, wherein the position indicates which of the plurality of volumes to access, wherein an offset is used to access volumes other than a first of the plurality of volumes; and means for, when the non-volatile data storage utilizes the second file system, operating the memory card in accordance with the second file system by accessing the entire address space of the non-volatile data storage as the single volume **[The subject matter of claim 51 is parallel to the subject matter of**

claim 39, except that it sets forth the claimed invention as an apparatus, and it is therefore rejected under the rationale in the rejection to claim 39 above. Claim 51 further requires means for determining ***(Identified in Applicant's Specification as "host controller" as "The memory card evaluation process 300 is, for example performed by a host controller within memory card" (pages 7-8, pars. 0037 and 0040; fig. 3); taught by the combination of Shinomura, Colligan and Suda as Shinomura discloses "PC card controller 18" (col. 13, lines 9-23; fig. 1 and related text) which comprises client device drivers 62 and 53 which determine whether the memory card utilizes a 16-bit or a 32-bit file system (col.16, lines 5-58; fig. 2 and related text))*** **means for, when the non-volatile storage utilizes the first file system, operating the memory card in accordance with first file system** ***(Identified in Applicant's Specification "controller 402" operating memory card for host access (fig. 4; pages 8-9, pars. 0042-0046); taught by the combination of Shinomura, Colligan and Suda as Shinomura disclose "PC card controller 18" (col. 13, lines 9-23; fig. 1 and related text) accessing "PC card" according to 16-bit file system (col. 10, line 61-col. 11, line 3))*** **, and mean for, when the non-volatile data storage utilizes the second file system, operating the memory card in accordance with the second file system** ***(Identified in Applicant's Specification as "controller 402" operating memory card for host access (fig. 4); pages 8-9, pars. 0042-0046); taught by the combination of Shinomura, Colligan and Suda as Shinomura discloses "PC card controller 18" (col. 13, lines 9-23; fig. 1 and related text) accessing "PC card" according to 16-bit file system (col. 10, line 61-col. 11, line 3) and as Suda discloses "controller 10" operating memory card (fig. 1 and related text; par. 0028))*** **].**

19. As per claim 52. (New) The apparatus of claim 51, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[The rationale in the rejection to claim 40 is herein incorporated]**.

20. As per claim 53. (New) The apparatus of claim 51, wherein the first file system is the FAT-16 file system **[The rationale in the rejection to claim 41 is herein incorporated]**.

21. As per claim 54. (New) The apparatus of claim 51, wherein the second file system is the FAT-32 file system **[The rationale in the rejection to claim 42 is herein incorporated]**.

22. As per claim 55. (New) The apparatus of claim 52, wherein each of the plurality of volumes has a maximum size of 2GB **[The rationale in the rejection to claim 43 is herein incorporated]**.

23. As per claim 56. (New) The apparatus of claim 51, wherein the means for determining includes means for accessing a portion of the non-volatile data storage stating which file system is utilized **[The rationale in the rejection to claim 44 is herein incorporated]**.

24. As per claim 57. (New) A program storage device readable by a machine, tangibly embodying a set of computer instructions executable by the machine for reading data from a memory card that provides non-volatile data storage having an address space defined by a contiguous range of addresses, the method comprising: determining whether the non-volatile data storage utilizes a first file system or a second file system; when the non-volatile data storage utilizes the first file system, operating the memory card in accordance with the first file system by: dividing the address space of the non-volatile

data storage into a plurality of volumes; formatting each of the plurality of volumes as a separate volume utilizing the first file system; accessing one of the plurality of volumes by determining a position of a physical switch, wherein the position indicates which of the plurality of volumes to access, wherein an offset is used to access volumes other than a first of the plurality of volumes; and when the non-volatile data storage utilizes the second file system, operating the memory card in accordance with the second file system by accessing the entire address space of the non-volatile data storage as the single volume **[The subject matter of claim 57 is parallel to the subject matter of claim 39, except that it sets forth the claimed invention as a program storage device embodying a set of instructions, and it is therefore rejected under the rationale in the rejection to claim 39 above]**.

25. As per claim 58. (New) The program storage device of claim 57, wherein the first file system utilizes 16 bit addressing and the second file system utilizes greater than 16 bit addressing **[The rationale in the rejection to claim 40 is herein incorporated]**.

26. As per claim 59. (New) The program storage device of claim 57, wherein the first file system is the FAT-16 file system **[The rationale in the rejection to claim 41 is herein incorporated]**.

27. As per claim 60. (New) The program storage device of claim 57, wherein the second file system is the FAT-32 file system **[The rationale in the rejection to claim 42 is herein incorporated]**.

28. As per claim 61. (New) The program storage device of claim 58, wherein each of the plurality of volumes has a maximum size of 2GB **[The rationale in the rejection to claim 43 is herein incorporated]**.

29. As per claim 62. (New) The program storage device of claim 57, wherein the determining includes accessing a portion of the non-volatile data storage stating which file system is utilized **[The rationale in the rejection to claim 44 is herein incorporated]**.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

30. Applicant's arguments filed on 10/15/2009 with respect to claims 39-62 have been fully considered but are moot in view of the new ground(s) of rejection. In these arguments, applicant relies on newly presented claims and argues previously presented references to Suda, Moro and Murray; however, all the argued limitations are taught by the new rejections presented above under Shinomura in view of Colligan and Suda. See rejections above.

CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

31. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

32. Per the instant office action, claims 39-62 have received an action on the merits and are subject of a non-final rejection.

a(2) CLAIMS NO LONGER UNDER CONSIDERATION

33. Claims 1-38 have been canceled as of amendment filed on 10/15/2009.

b. DIRECTION OF FUTURE CORRESPONDENCES

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

35. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 2, 2009

/Yaima Campos/
Examiner, Art Unit 2185